EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	1	1 AND ((BMC "bounded model checking" bounded$1model $1checking) WITH (loop looped looping iteration iterate iterating iterated iterative feedback feed $1back))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 11:45
L7	2	1 AND ((abstract abstracted abstraction abstracting reduce reduced reducing reduction decrease decreased decreasing shrink shrinking shrunk condense condensed condensing compress compressed compressing compression simplify simplified simplifying simplification) WITH (satisfiability SAT satisfiable))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 11:43
L6	0	1 AND (((design model circuit) near2 (abstract abstracted abstraction abstracting reduce reduced reducing reduction decrease decreased decreasing shrink shrinking shrunk condense condensed condensing compress compressed compressing compression simplify simplified simplifying simplification)) WITH (satisfiability SAT satisfiable))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 11:43

L5	0	1 AND ((ID identification identify identified identifying tag tagged tagging Markup Mark$1up Mark Marked Marking label labeled labelled labeling labelling name named naming) WITH (assertion asserting assert asserted checker constraint property (boolean ADJ expression) (logical ADJ expression) condition (Sentry ADJ (verifi$6 verify$3) ADJ (check$2 entity)) (logic ADJ checking) logic $1checking) WITH (satisfiability SAT satisfiable))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 11:41
L4	9	3 AND ((node logic net wire cell) WITH (assertion asserting assert asserted checker constraint property (boolean ADJ expression) (logical ADJ expression) condition (Sentry ADJ (verifi$6 verify$3) ADJ (check$2 entity)) (logic ADJ checking) logic $1checking))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 11:38
L3	13	1 AND ((ID identification identify identified identifying tag tagged tagging Markup Mark$1up Mark Marked Marking label labeled labelled labeling labelling name named naming) WITH (assertion asserting assert asserted checker constraint property (boolean ADJ expression) (logical ADJ expression) condition (Sentry ADJ (verifi$6 verify$3) ADJ (check$2 entity)) (logic ADJ checking) logic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 11:33

		$1checking))				
L2	4	1 AND ((ID identification identify identified identifying tag tagged tagging Markup Mark$1up Mark Marked Marking label labeled labelled labeling labelling name named naming) WITH (sequential latch flip $1flop (flip ADJ flop) register))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 11:27
L1	22	("20030208730" | "5465216" | "5724504" | "6102959" | "6192505" | "6292765" | "6311293" | "6356858" | "6408262" | "6751582").PN. OR ("6848088").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/08 11:26
S117	13	S114 AND (BMC "bounded model checking" bounded $1model$1checking)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/06 19:12
S116	13	S114 AND (abstract abstracted abstraction abstracting reduce reduced reducing reduction decrease decreased decreasing shrink shrinking shrunk condense condensed condensing compress compressed compressing compression simplify simplified simplifying simplification)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/06 19:07

S114	13	(US-20080134115-$ or US-20080066032-$ or US-20050268265-$ or US-20050240885-$ or US-20050081169-$ or US-20040230407-$). did. or (US-6848088-$ or US-7552407-$ or US-7454324-$ or US-7373624-$ or US-7356789-$ or US-7318205-$ or US-7305637-$).did.	US-PGPUB; USPAT	OR	ON	2010/04/06 19:07
S113	13	S112 AND (cone WITH (sequential latch flip $1flop (flip ADJ flop) register))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/06 19:02
S112	26	S111 AND (satisfiability SAT) AND (BMC "bounded model checking" bounded $1model$1checking)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/06 19:01
S111	2007	(design model circuit) AND (abstract abstracted abstraction abstracting reduce reduced reducing reduction decrease decreased decreasing shrink shrinking shrunk condense condensed condensing compress compressed compressing compression simplify simplified simplifying simplification) AND (fanin fan$1in) AND (sequential latch flip $1flop (flip ADJ flop) register)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/06 19:01
S110	3	S109 AND (satisfiability SAT) AND (BMC "bounded model checking" bounded $1model$1checking)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/06 19:01

S109	129	(design model circuit) SAME (abstract abstracted abstraction abstracting reduce reduced reducing reduction decrease decreased decreasing shrink shrinking shrunk condense condensed condensing compress compressed compressing compression simplify simplified simplifying simplification) SAME (fanin fan$1in) SAME (sequential latch flip $1flop (flip ADJ flop) register)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/06 19:01

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L16	2	14 AND loop.clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/08 15:41
L15	1	14 AND (fanin fan$1in). clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/08 15:41
L14	37	(satisfiability SAT).clm. AND (BMC "bounded model checking" bounded$1model $1checking).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/08 15:41
L13	1	11 AND (fanin fan$1in). clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/08 15:36
L12	0	11 AND loop.clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/08 15:36

L11	16	(abstract abstracted abstraction abstracting reduce reduced reducing reduction decrease decreased decreasing shrink shrinking shrunk condense condensed condensing compress compressed compressing compression simplify simplified simplifying simplification).clm. AND (satisfiability SAT).clm. AND (BMC "bounded model checking" bounded$1model $1checking).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/08 15:35
L10	2	(design model circuit).clm. SAME (abstract abstracted abstraction abstracting reduce reduced reducing reduction decrease decreased decreasing shrink shrinking shrunk condense condensed condensing compress compressed compressing compression simplify simplified simplifying simplification).clm. SAME (fanin fan$1in).clm. SAME (sequential latch flip$1flop (flip ADJ flop) register).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/08 15:16
L9	30	(design model circuit).clm. AND (abstract abstracted abstraction abstracting reduce reduced reducing reduction decrease decreased decreasing shrink shrinking shrunk condense condensed condensing compress compressed compressing compression simplify simplified simplifying simplification).clm. AND (fanin fan$1in).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/08 15:15

		AND (sequential latch flip$1flop (flip ADJ flop) register).clm.				

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